

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of Claims:**

1. (Currently amended) A system comprising:  
a plurality of memory bus masters, each to generate an independent clock signal on respective outputs, each of said outputs connected by a transmission line to a common node, said common node additionally connected to a plurality of clock inputs of a memory array; and  
an isolation circuit coupled between each of said transmission lines and said common node, the isolation circuit including a switching device coupled to a respective transmission line and a corresponding respective control input, the respective control input to select or de-select the respective transmission line for input to the memory array.
2. (Currently amended) The system of claim 1, ~~further comprising control inputs connected to said isolation circuit, to~~ wherein the control inputs select one of said plurality of memory bus masters to drive a corresponding clock signal to said memory array while isolating the transmission lines of the other bus masters from said common node.
3. (Original) The system of claim 2, wherein said control inputs are supplied by a memory bus arbiter.
4. (Original) The system of claim 1, wherein said isolation circuit places a high impedance between said common node and said transmission lines.

5. (Original) The system of claim 1, wherein said isolation circuit comprises a plurality of FETs.

6. (Original) The system of claim 1, wherein said isolation circuit is a multiplexer.

7. (Currently amended) In a computer board layout including a memory array and plurality of memory bus masters, a method comprising:

connecting each of said bus masters to a common node via a transmission line;

connecting said memory array to said common node; and

placing an isolation circuit between each of said transmission lines and said common node ;

in the isolation circuit, pairing each of the transmission lines with a corresponding respective control input to select one of said bus masters to drive a clock input to said memory array while isolating the transmission lines of the other bus masters from said common node.

8. (Canceled)

9. (Currently amended) A circuit comprising:

a plurality of transmission lines coupled between respective bus master clock outputs and a common node;

a plurality of memory modules coupled to said common node; and

an isolation circuit coupled between said plurality of transmission lines and said common node, the isolation circuit including a switching device coupled to a respective transmission line and a corresponding respective control input, the

respective control input to select or de-select the respective transmission line for input to the memory modules.

10. (Currently amended) The circuit of claim 9, further comprising:  
~~control means connected to said isolation circuit, said control means being configured to~~ bus arbiter means to determine values of the control inputs to  
select one of said bus master clock outputs to drive to said memory modules,  
while selecting the transmission lines associated with the other bus master clock  
signals for isolation from said common node.

11. (Original) The circuit of claim 9, wherein a clock input of each of said  
memory modules is connected to said common node.

12. (Original) The circuit of claim 9, where said memory modules are  
SDRAM modules.

13. (Currently amended) A method comprising:  
connecting transmission lines from a plurality of memory bus masters to a  
common node;  
connecting a memory array to said common node;  
pairing each of the transmission lines with a corresponding respective  
control input to select one of said bus masters to drive a clock input to said  
memory array while isolating the transmission lines of the other bus masters from  
said common node  
selecting one of said memory bus masters to drive clock outputs to said  
memory array by asserting a corresponding respective control input; and  
introducing a high impedance between the transmission lines of the other  
memory bus masters and said common node by asserting the other control  
inputs.

14. (Currently amended) The method of claim 13, wherein said selected ~~bus master is selected by~~ control inputs are from a memory bus arbiter.

15. (Original) The method of claim 13, wherein said high impedance comprises FETs.